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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,279	11/19/2003	Steven J. Koester	YOR920030533US1 (17110)	7401

23389 7590 04/26/2006

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EXAMINER	
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ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,279	KOESTER, STEVEN J.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *10-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed February 13, 2006 has been entered. Claim 1 has been amended. Non-elected invention, claims 10-21 have been withdrawn. Claims 1-21 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

SEMICONDUCTOR FIELD-EFFECT TRANSISTOR HAVING STRAINED-LAYER.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

Line 6 recites: "said source and drain *electrodes*", the correct term should be: "said source and drain *regions*".

Appropriate correction is required.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, *the first layer comprises a multi-layer structure* (claim 3) and *first layer comprises a relaxed substrate* (claim 4) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein said *first layer* of semiconductor material comprises a *SiGe relaxed substrate*" (claim 4) in the application as filed.

Note that, the limitation of claim 1, lines 2-3, includes: a first layer of semiconductor material doped of a first dopant type formed on a substrate.

Since first layer and substrate are separated, thus first layer can not comprise a SiGe relaxed substrate.

Applicants must cancel or provide support for the new matter.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites: "wherein said *first layer* of semiconductor material comprises a *SiGe relaxed substrate*".

Since the first layer is formed on the substrate, thus, the first layer can not comprise a substrate.

Therefore, claim 4 is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5 is rejected under 35 U.S.C. 102(b) as being anticipated by Takase et al. (JP. Patent No. 11-087706).

With respect to claim 1, Takase teaches a semiconductor field-effect transistor device as claimed including:

a first layer (layer above line 185) of semiconductor material doped of a first dopant type (p) formed on a substrate (100);

a source region and a drain region (180) implanted with dopants of a second opposite type (n);

a gate electrode (170) separated from the first layer by a dielectric region (140), and positioned between the source and drain regions (180);

the substrate having one or more dislocation or crystal defects (185) that extends continuously from the source region to the drain region (180), and

blocking impurity dopant materials (In^+) that partially or fully occupies the dislocation defects (185), wherein the blocking impunity dopant materials substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocations or crystal defect (185). (See Fig. 1e).

With respect to claim 2, the first layer of semiconductor material of Takase comprises material selected from the group comprising: Si.

With respect to claim 3, the first layer of semiconductor material (Si layer above the line 185) of Takase comprises multi-layer structure comprising material selected from the group comprising Si.

It is well known in the art that a thick silicon layer is seen as multitude of mono-layers of silicon.

The Examiner takes Official Notice of the equivalence of a thick silicon layer and a multi-layer of mono-layer of silicon for their use in the art of semiconductor apparatus and the selection of any of these known equivalents to be used as a channel layer would be within the knowledge of ordinary skill in the art.

With respect to claim 4, as best understood by the examiner, the first layer of semiconductor material of Takase is formed on a substrate.

With respect to claim 5, the source and drain dopants of the second type of Takase comprises P, As, singly or combination thereof and the blocking impurity is In.

8. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Shahidi et al., A High Performance 0.15 μm CMOS. VLSI. Tech. Symp. Dig. 1993 , pp. 93-94.

With respect to claim 1, Shahidi teaches a semiconductor field-effect transistor device, Fig. 2, as claimed including:

a first layer (layer above the darkened line) of semiconductor material doped of a first dopant type (p or n) formed on a substrate (p-well or n-well);

a source region and a drain region (n^+ or p^+) implanted with dopants of a second opposite type (n or p);

a gate electrode separated from the first layer by a dielectric region, and positioned between the source and drain regions;

the substrate (p-well or n-well) having one or more dislocation or crystal defects (darkened line) that extends continuously from the source region to the drain region, and

blocking impurity dopant materials (In or Sb) that partially or fully occupies the dislocation defects, wherein the blocking impunity dopant materials substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocations or crystal defect. (See Fig. 2).

With respect to claim 2, the first layer of semiconductor material of Shahidi comprises material selected from the group comprising: Si.

With respect to claim 3, the first layer of semiconductor material of Shahidi comprises multi-layer structure comprising material selected from the group comprising Si.

It is well known in the art that a thick silicon layer is seen as multitude of mono-layers of silicon.

The Examiner takes Official Notice of the equivalence of a thick silicon layer and a multi-layer of mono-layer of silicon for their use in the art of semiconductor apparatus and the

selection of any of these known equivalents to be used as a channel layer would be within the knowledge of ordinary skill in the art.

With respect to claim 4, as best understood by the examiner, the first layer of semiconductor material of Shahidi is formed on a substrate.

With respect to claim 5, the source and drain dopants of the second type of Shahidi comprises P, As, singly or combination thereof and the blocking impurity is In.

With respect to claim 6, the source and drain dopants of the second type of Shahidi comprises B singly or combination thereof and the blocking impurity is Sb.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase '706 or Shahidi et al., as applied to claim 1 above, and further in view of Eimori (U.S. Patent No. 5,245,208).

With respect to claim 7, Takase or Shahidi a semiconductor field-effect transistor as described in claim 1 above including blocking impurity.

Thus, Takase and Shahidi are shown to teach all the features of the claim with the exception of utilizing a neutral species for the blocking impurity.

However, Eimori teaches a semiconductor field-effect transistor including a blocking impurity dopant material (8a) utilizing a neutral-type impurity. (See Fig. 5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the blocking impurity material of Takase or Shahidi utilizing neutral-type impurity as taught by Eimori to reduce hot carriers effect.

With respect to claim 8, the blocking impurity (Ge) of Eimori is group IV impurity.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takase '706 or Shahidi et al. and Eimori '208 as applied to claim 7 above, and further in view of Gardner et al. (U.S. Patent No. 5,969,407).

Takase or Shahidi and Eimori are shown to teach all the features of the claim with the exception of specifically utilize other species of group IV impurity for the neutral-type impurity.

However, Gardner teaches other impurities of group IV impurity such as silicon (Si) or carbon (C) are known to be used interchangeably for the purpose.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the blocking impurity material of Takase or Shahidi and Eimori utilizing other impurity of group IV as taught by Gardner since they can be used interchangeably.

Response to Arguments

11. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER